AMENDMENTS TO THE CLAIMS

1. (Currently amended) A stack package including two or more area array type chip scale packages, each chip scale package comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate;

a plurality of circuit patterns formed on the lower surface of the substrate and electrically connected to the ball land pads; and

one or more chips installed on an upper surface of the substrate and electrically connected to the circuit patterns,

wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner where the ball land pads of the upper stacked chip scale package face the opposite direction as the ball land pads of the lower stacked chip scale packages, and wherein the circuit patterns on the lower surface of the substrate of the upper stacked chip scale package are electrically connected to ~~those~~ the circuit patterns on the lower surface of the substrate of the lower stacked chip scale package.

2. (Original) The stack package according to claim1, wherein the circuit patterns of the upper stacked chip scale package are electrically connected to the circuit patterns of the lower stacked chip scale package by connecting boards.

3. (Original) The stack package according to claim 2, wherein each connecting board comprises a flexible film and wiring patterns formed on the film.

4. (Original) The stack package according to claim 1, wherein a hole is formed in the substrate of each chip scale package, and the chip is electrically connected to the circuit patterns by bonding wires passing through the hole.

5. (Original) The stack package according to claim 4, wherein a plurality of bonding pads of each chip scale package are formed on the central region of the chip and exposed through the hole, and wherein one end of each bonding wire is attached to a corresponding bonding pad of the chip.

6. (Original) The stack package according to claim 5, wherein the chip is protected by a first encapsulating part, and the bonding pads and the bonding wires are protected by a second encapsulating part.

7. (Original) The stack package according to claim 6, wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other by an adhesive applied on the first encapsulating part.

8. (Original) The stack package according to claim 1, wherein a plurality of solder balls is formed on the ball land pads of the lowest stacked chip scale package.

9. (Original) The stack package according to claim 1, wherein a single chip scale package is stacked on, and electrically connected through a plurality of solder balls to adjacently stacked chip scale packages coupled by connecting boards.

10. (Original) The stack package according to claim 1, wherein an adjacently stacked chip scale packages coupled by connecting boards are stacked on, and electrically connected through a plurality of solder balls to another adjacently stacked chip scale packages coupled by connecting boards.

11. (Original) The stack package according to claim 1, wherein a plurality of connection pads are formed on the outside of the region of the substrate on which a plurality of ball land pads are formed, and electrically connected to the circuit patterns.

12. (Original) The stack package according to claim 11, wherein connecting boards are electrically connected to the circuit patterns through the connection pads.

13. (Original) The stack package according to claim 12, wherein both ends of the connecting board at which the connecting board is attached to the connection pads are bent.

14-20. (Cancelled)

21. (New) A stack package comprising:
a first area array type chip scale package; and

a second area array type chip scale package,

wherein the first and second chip scale packages have substantially a same width and substantially a same length, each chip scale package comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate; and

one or more chips installed on an upper surface of the substrate,

wherein the lower surfaces of the substrates of the chip scale packages face the opposite direction.

22. (New) The stack package of claim 21, wherein each chip scale package includes a circuit pattern formed on the lower surface of the substrate that is electrically connected to the ball land pads, and

the circuit patterns on the two chip scale packages are electrically connected.

23. (New) The stack package of claim 22, wherein the circuit patterns on the two chip scale packages are electrically connected by connecting boards.

24. (New) The stack package of claim 21, further comprising a plurality of solder balls formed on the ball land pads of the first chip scale package.

25. (New) The stack package of claim 24, further comprising a third chip scale package having substantially a same width and substantially a same length as the first and second chip scale packages,

wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls formed on a plurality of ball land pads on a lower surface of a substrate of the third chip scale package.

26. (New) The stack package of claim 24, further comprising:

a third chip scale package; and

a fourth chip scale package,

wherein the third and fourth chip scale packages have substantially a same width and substantially a same length as the first and second chip scale packages, the third and fourth chip scale packages comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate; and

one or more chips installed on an upper surface of the substrate,

wherein the lower surfaces of the substrates of the third and fourth chip scale packages face the opposite direction,

wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls formed on the ball land pads of the third chip scale package.